Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 2, with the following amended paragraph:

This invention relates generally to capacitive [[of]] micromachined ultrasonic transducers (cMUTs) and more particularly to [[a]] capacitive micromachined ultrasonic transducers having a patterned isolation layer which prevents shorting of the electrodes during operation and reduces the total number of trapped charges as compared to a non-patterned isolation layer.

Please replace the paragraph beginning at page 1, line 7, with the following amended paragraph:

Ultrasonic transducers have been used in a number of sensing applications such as medical imaging, non-destructive evaluation, gas metering and a number of ultrasound generating application such medical therapy, industrial cleaning, etc. One class of such transducers is the electrostatic transducers. Electrostatic transducers have long been used for receiving and generating acoustic waves. Large area electrostatic transducer arrays have been use for acoustic imaging. The electrostatic transducers employ resilient membranes with very little inertia substrate which forms the second electrode. When distances between the electrodes are small the transducers can exert very large forces against a fluid in contact with the membrane. The momentum carried by approximately half a wavelength of air molecules in contact with the upper surface is able to set the membrane in motion and vice versa. Electrostatic actuation and detection enables the realization and control of such membranes.

Please replace the paragraph beginning at page 3, line 21, with the following amended paragraph:

An example of a process for forming cMUT with cells including isolation posts or areas is shown and described with regard to Figures 3A-3G. For example, the process may start with an n type silicon wafer 21 Figure 3A. The wafer can be heavily doped as, for example, with

antimony to achieve a low resistance, for example, in the range of 0.008 to 0.020 ohm-centimeters square. Depending on the required electrodes separation of the cMUT one or two different processes form shallow or deep cavities before wafer bonding. When the separation distance between electrodes is less than two micrometers one can use a thermal oxide layer which is etched to form the cavity. A layer 22 of thermal oxide is grown and patterned using convention photolithography and etched to define the wells 23. If the depth of the wells 23 is to be larger than 2 micrometers the wafer is processed by selectively etching the silicon substrate 21 at the bottom of the wells to increase the depth. After the wells have been formed another thermal oxide layer is grown and patterned using conventional photolithography to leave oxide posts or areas 24 at the bottom of the wells, Figure 3B. It should be understood that the areas can be patterned to have any size and shape. The height of the posts or areas is determined by the thickness of the oxide layer. The wafer with cavities is then bonded to a SOI wafer 26 under vacuum as shown in Figure 3C. Water bonding can be done with a bonder at approximately $1x10^{-5}$ microbar vacuum at 150 degrees. The bonded wafers are annealed at 1100 degrees centigrade for two hours. The wafer is ground and etched back through the oxide layer 27 leaving a silicon membrane 28. The active silicon layer 28 on the SOI wafer now constitutes the membrane 28 for the cMUT transducer. The thickness of the active silicon layer 28 becomes the membrane thickness and can be easily controlled. To gain electrical access to the carrier silicon wafer 21 openings 29 in the membrane, silicon and insulating silicon oxide layer [[is]] <u>are</u> formed by masking and etching. Subsequently a thin film of aluminum 31 is sputtered and patterned to establish a connection to the top electrodes and to the substrate. A thin layer of low temperature oxide 32 then is deposited as a passive layer. Finally, the low temperature oxide layer is patterned and etched to create pads 33 for wire bonding.